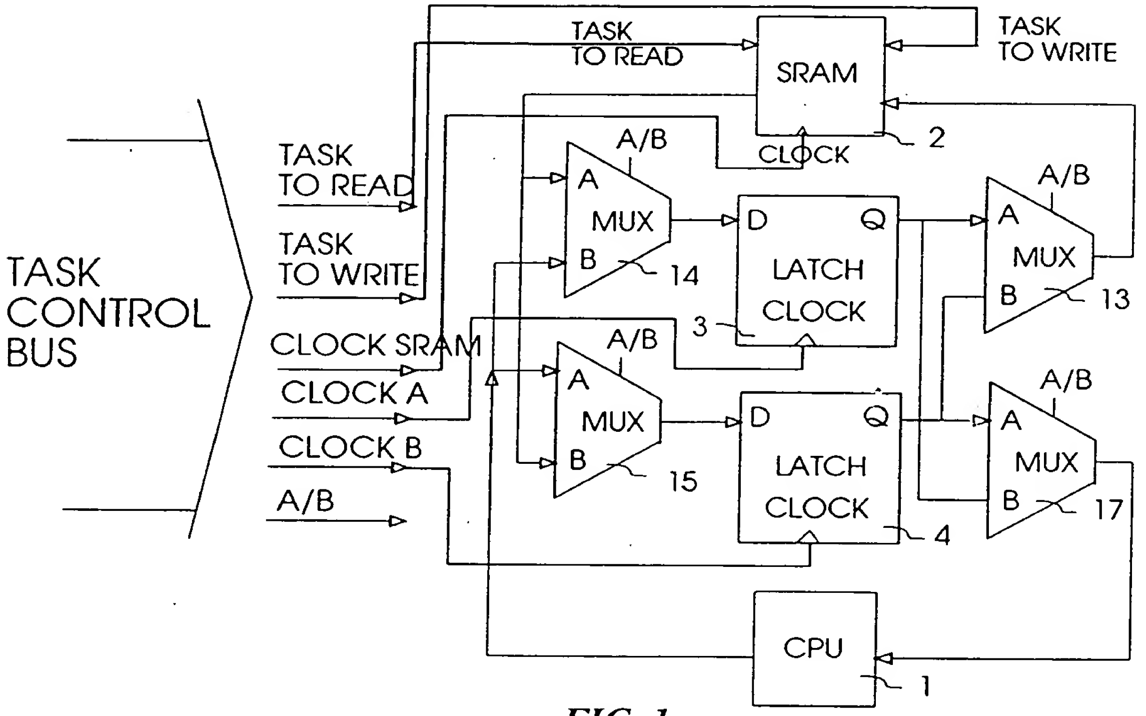
TASK CONTROL BUS
TASK TO READ
TASK TO WRITE
CLOCK SRAM
CLOCK A
CLOCK B
A/B
TASK TO READ
SRAM
TASK TO WRITE
CLOCK
2
A/B
A
MUX
B
14
D
Q
LATCH
CLOCK
3
A/B
A
MUX
B
13
A/B
A
MUX
B
15
D
Q
LATCH
CLOCK
4
A/B
A
MUX
B
17
CPU
1

FIG. 1

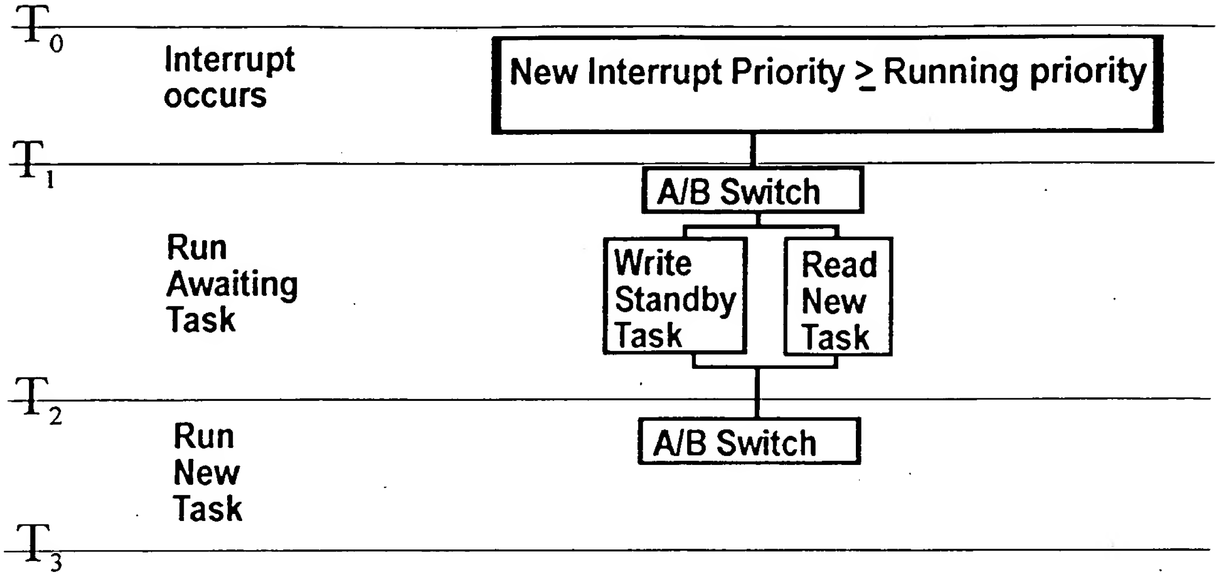
T_0
Interrupt occurs
New Interrupt Priority ≥ Running priority
T_1
A/B Switch
Run Awaiting Task
Write Standby Task
Read New Task
T_2
Run New Task
A/B Switch
T_3

Fig. 2

Set Interrupt Enable latch if: Link Register task decoder asserted & LINKED

Clear Interrupt Enable latch IEL if: Link register task decoder & not LINKEED, and write
or: Running task decoder asserted & LINKED

Fig. 3A

LINKED	write	Link register	Run task	Set/Clear IEL
1	0	1	0	SET
0	1	1	0	CLEAR
1	0	0	1	CLEAR
		Everything Else		Nothing

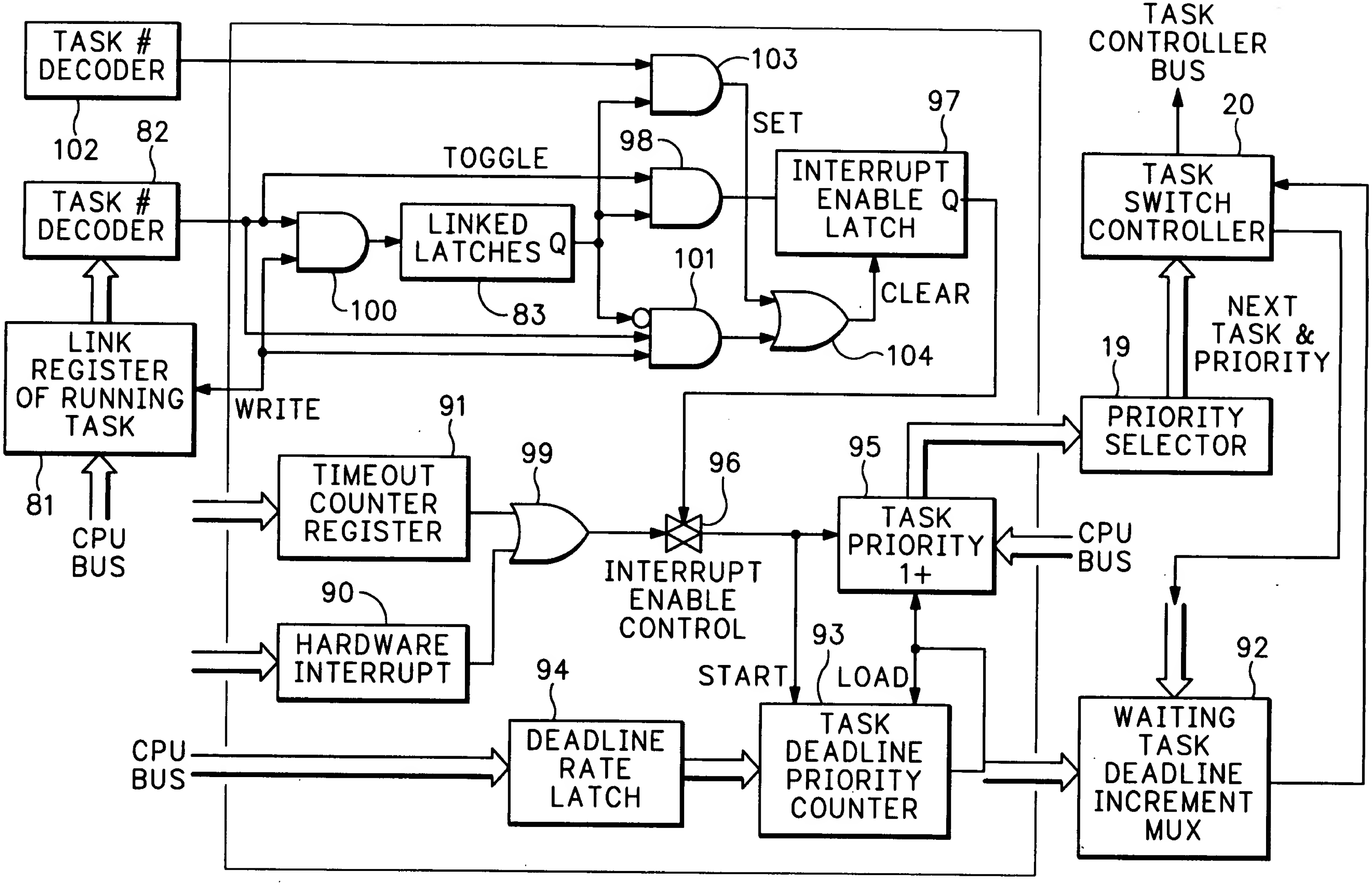
TASK # DECODER
102
82
TASK # DECODER
LINK REGISTER OF RUNNING TASK
81
CPU BUS
WRITE
TOGGLE
100
LINKED LATCHES Q
83
103
SET
98
101
97
INTERRUPT ENABLE Q LATCH
CLEAR
104
91
TIMEOUT COUNTER REGISTER
99
90
HARDWARE INTERRUPT
96
INTERRUPT ENABLE CONTROL
94
DEADLINE RATE LATCH
CPU BUS
START
93
LOAD
TASK DEADLINE PRIORITY COUNTER
95
TASK PRIORITY 1+
CPU BUS
PER TASK
TASK CONTROLLER BUS
20
TASK SWITCH CONTROLLER
NEXT TASK & PRIORITY
19
PRIORITY SELECTOR
92
WAITING TASK DEADLINE INCREMENT MUX

Fig.3

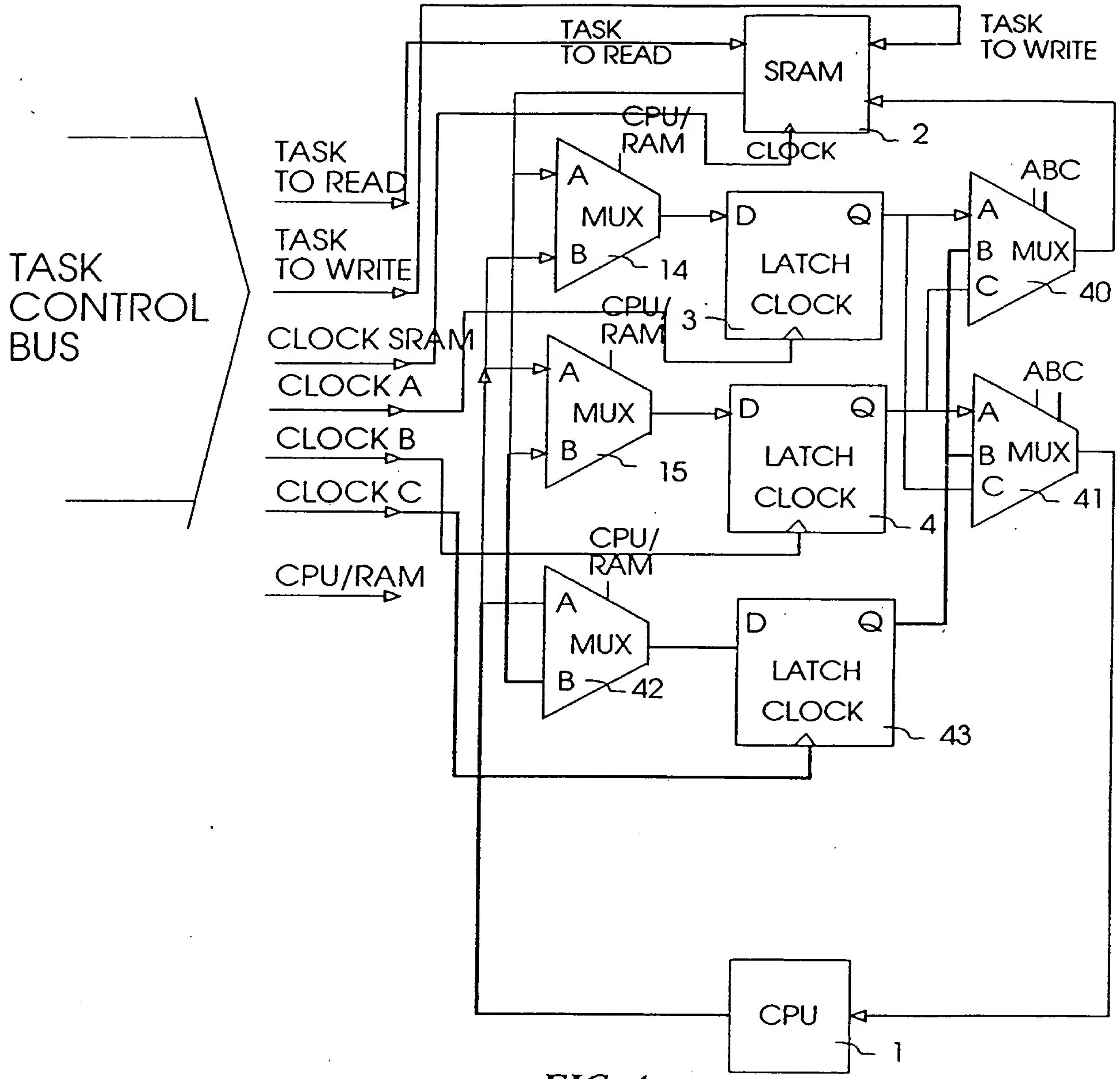
TASK CONTROL BUS
TASK TO READ
TASK TO WRITE
CLOCK SRAM
CLOCK A
CLOCK B
CLOCK C
CPU/RAM
TASK TO READ
SRAM
TASK TO WRITE
CLOCK
2
CPU/ RAM
A
MUX
B
14
D
Q
LATCH
CLOCK
3
CPU/ RAM
A
MUX
B
15
D
Q
LATCH
CLOCK
4
CPU/ RAM
A
MUX
B
42
D
Q
LATCH
CLOCK
43
ABC
A
B MUX
C
40
ABC
A
B MUX
C
41
CPU
1

FIG. 4

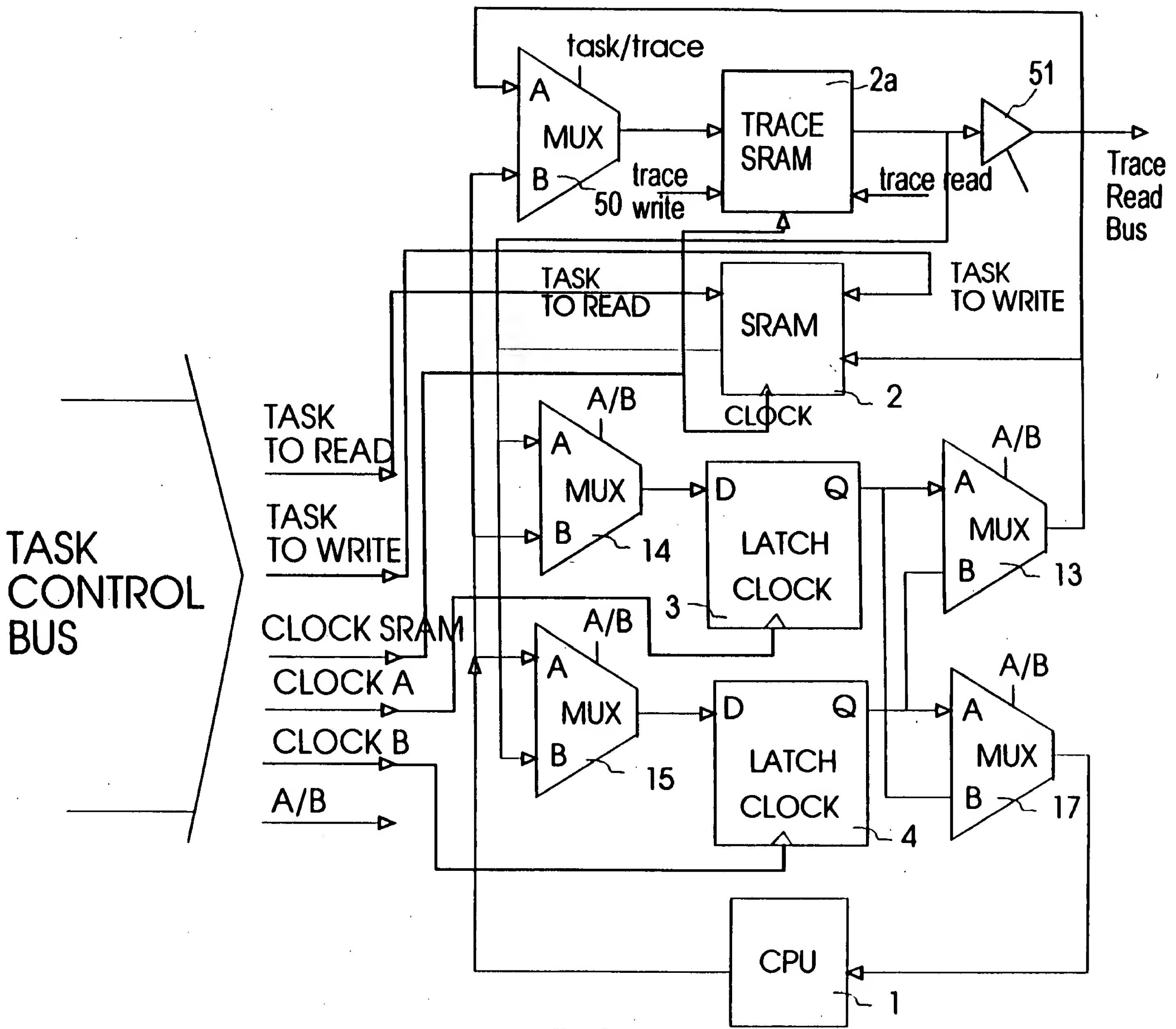
task/trace
A
MUX
B
50
trace write
TRACE SRAM
2a
trace read
51
Trace Read Bus
TASK TO READ
SRAM
TASK TO WRITE
CLOCK
2
TASK CONTROL BUS
TASK TO READ
TASK TO WRITE
CLOCK SRAM
CLOCK A
CLOCK B
A/B
A/B
A
MUX
B
14
D
Q
LATCH
CLOCK
3
A/B
A
MUX
B
13
A/B
A
MUX
B
15
D
Q
LATCH
CLOCK
4
A/B
A
MUX
B
17
CPU
1

FIG. 5

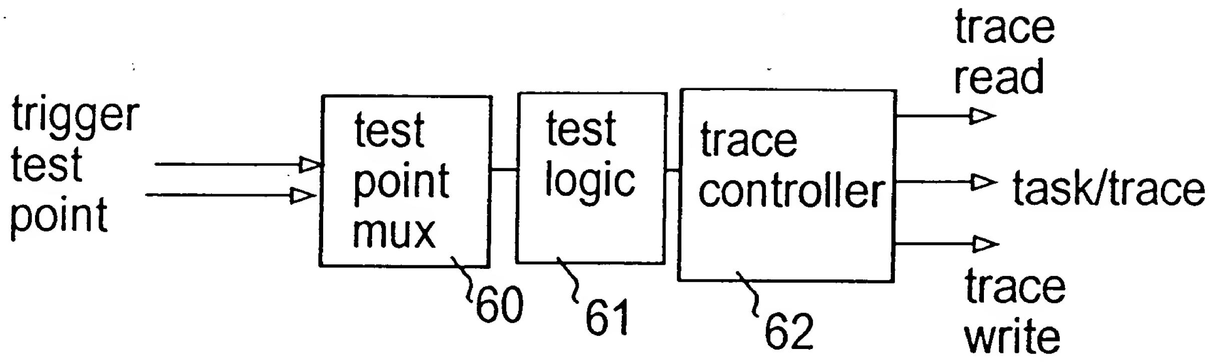
trigger
test
point
test
point
mux
60
test
logic
61
trace
controller
62
trace
read
task/trace
trace
write

FIG. 6

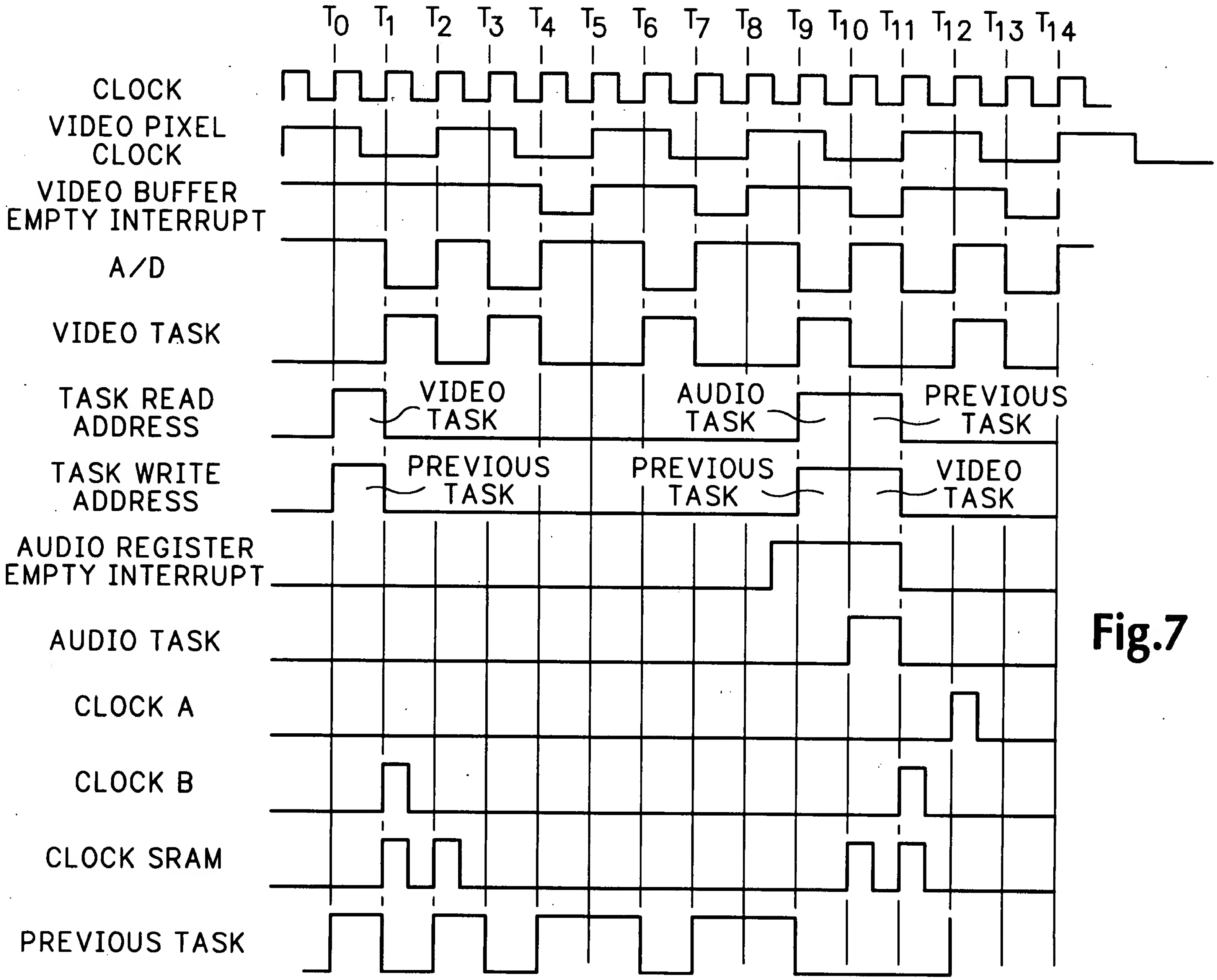
T0
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
T11
T12
T13
T14
CLOCK
VIDEO PIXEL CLOCK
VIDEO BUFFER EMPTY INTERRUPT
A/D
VIDEO TASK
TASK READ ADDRESS
VIDEO TASK
AUDIO TASK
PREVIOUS TASK
TASK WRITE ADDRESS
PREVIOUS TASK
PREVIOUS TASK
VIDEO TASK
AUDIO REGISTER EMPTY INTERRUPT
AUDIO TASK
CLOCK A
CLOCK B
CLOCK SRAM
PREVIOUS TASK

Fig.7